

## REMARKS/ARGUMENTS

Claims 1-17 and 41-45 are currently pending in the present patent application, with claims 18-40 having been withdrawn by the Examiner.

In an Office Action mailed on October 18, 2005, the Examiner rejected claims 1-5 and 9-11 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent Application Publication No. 2004/0142542 A1 to Murphy *et al.* ("Murphy"). Claims 6-8, 12, 13, 14-17, 41-45 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Murphy in view of various combinations of U.S. Patent No. 5,322,811 to Komuro *et al.* ("Komuro") and U.S. Patent No. 6,033,928 to Eriguchi *et al.* ("Eriguchi").

Before addressing the Examiner's rejections of the claims, the disclosed embodiments of the invention will first be discussed in comparison to the applied references in order to help the Examiner appreciate certain distinctions between the pending claims and the subject matter of the applied references. Specific distinctions between the pending claims and the applied references will be discussed after the discussion of the disclosed embodiments and the applied references. This discussion of the differences between the disclosed embodiments and applied references does not define the scope or interpretation of any of the claims.

Figures 10-15 of the application illustrate an embodiment of the present invention. As shown in Figure 10, trenches 8 are formed in a semiconductor substrate 7, or alternatively cylindrical trenches 10 are formed in the substrate as shown in Figure 11. This structure is annealed and through migration of the material of the substrate 7 spherical cavities 10a are formed as shown in Figure 12. A semiconductor layer 9 is formed on this structure after the annealing as shown in Figure 12. As shown in Figure 13, trenches 11 orthogonal to the spherical cavities 10a or microchannels 10b are then formed in the semiconductor layer 9. These trenches 11 are deep enough to intersect with the microchannels 10b. An electro-chemical process as discussed in paragraphs 73-78, for example, is then performed on this structure to convert a crystalline silicon layer containing the microchannels 10b into a porous silicon layer 12 as shown in Figure 14.

This porous silicon layer 12 is then oxidized as shown in Figure 15 to form dielectric layer 12a that isolates the substrate 7 from the layer 9. The trenches 11 in the layer 9 are then filled with a dielectric and desired devices formed in the layer 9.

Murphy discloses a different process that does happen to include forming buried cavities in a substrate, but for an entirely different purpose and with a different resulting structure. Figure 1a of Murphy shows a substrate 1 in which trenches 2 are formed and thereafter as shown in Figure 1b the structure is heated to form closed layer 4 and the buried cavities 3. These buried cavities 3 are ultimately used as a “separation layer” to allow separation of a structure formed above the cavities from the substrate 1 below the cavities. As shown in Figure 2c, a continuous cavity 7 is formed from the trenches 3 shown in Figure 2bc to separate a carrier wafer 5 and oxide layer 6 attached to the closed layer 4. This results in the structure including the carrier wafer 5, oxide layer 6, and then the semiconductor layer 4, which has a smooth surface 4a (Figure 4) and in which desired devices are formed.

Claim 1 recites a SOI-type semiconductor substrate including at least a buried insulating cavity formed according to the steps forming on the semiconductor substrate a plurality of trenches and forming a surface layer on the semiconductor substrate in order to close superficially the plurality of trenches. The method further includes forming, in the meantime, the at least one cavity buried in correspondence with the surface-distal end of the trenches. A first semiconductor material layer is formed on the surface layer with the same concentration as the semiconductor substrate wherein at least a trench is formed which is in communication with the at least one buried cavity.

Murphy neither discloses nor suggest the SOI-type semiconductor substrate recited in claim 1. There is no first semiconductor material layer formed on the surface layer with the same concentration as the semiconductor substrate wherein at least a trench is formed which is in communication with the at least one buried cavity. In Murphy, no trenches are formed in the layer 4 in communication with the buried cavities 3 or continuous cavity 7. The same is true for the wafer 5 and oxide layer 6. Moreover, there is no suggestion to do so in Murphy since the buried cavities 3/cavity 7 are used as a separation layer and not as an isolation layer as in present application and as in the structure recited in claim 1.

For these reasons, the combination of elements recited in amended claim 1 is allowable and dependent claims 2-8 are allowable for at least the same reasons as claim 1 and due to the additional limitations added by these claims.

Amended claim 9 recites suspended membrane formed on a semiconductor substrate of a first type of concentration and comprising at least a buried insulating cavity formed through the steps of forming on said semiconductor substrate a plurality of trenches, and performing an annealing step in a non-oxidizing atmosphere on all said semiconductor substrate up to form a surface layer on said semiconductor substrate in order to close superficially said plurality of trenches forming in the meantime said at least one buried cavity in correspondence with the surface-distal end of said trenches. The surface layer forms the membrane, and a first semiconductor material layer is formed on the surface layer with at least one trench being formed in the first semiconductor material layer which intersects with at least one of the buried cavities.

Once again, Murphy neither discloses nor suggests the suspended membrane structure recited in amended claim 9. There is no first semiconductor material layer formed on the surface layer with at least one trench being formed which intersects with the at least one of the buried cavities. In Murphy, no trenches are formed in the layer 4 in communication with the buried cavities 3 or continuous cavity 7 or the wafer 5 and oxide layer 6. There is no suggestion to do so in Murphy since the buried cavities 3/cavity 7 are used as a separation layer and not as an isolation layer as in present application and as in the structure recited in claim 9. The combination of elements recited in amended claim 9 is accordingly allowable, and dependent claims 10-13 are allowable for at least the same reasons as claim 9.

Amended claim 14 recites a MOSFET transistor integrated on a semiconductor substrate of a first type of concentration and comprising at least one buried insulating cavity formed through the steps of forming on said semiconductor substrate a plurality of trenches and performing an annealing step in a non-oxidizing atmosphere on all said semiconductor substrate up to form a surface layer on said semiconductor substrate in order to close superficially said plurality of trenches. At least one buried cavity is formed in correspondence with the surface-distal end of said trenches and a first semiconductor material layer is formed on the surface layer with at least one trench being formed in the

first semiconductor material layer which is in communication with said at least one buried cavity. The at least one buried insulating cavity forms at least part of the channel region of said MOSFET transistor.

The Murphy patent neither discloses nor suggests the MOSFET transistor recited in amended claim 14. There is no first semiconductor material layer formed on the surface layer with at least one trench being formed in the first semiconductor material layer which is in communication with said at least one buried cavity and with the at least one buried insulating cavity forming at least part of the channel region of said MOSFET transistor. As discussed above with regard to claims 1 and 9, there is no reason to do so given the goals of the Murphy patent. Neither does Komuro disclose or suggest such a structure. Accordingly, the combination of elements recited in amended claim 14 is allowable and dependent claims 15-17 are allowable for at least the same reasons as claim 14.

Amended claim 41 recites a semiconductor structure including a first portion of a semiconductor substrate, a cavity disposed in the first portion of the semiconductor substrate, and a second portion of the semiconductor substrate disposed over the cavity. At least one trench is formed in the second portion of the semiconductor substrate, each trench adjoining the cavity. A device is disposed in the second portion of the semiconductor substrate. Neither Murphy nor Komuro, whether taken singly or in combination, discloses or suggests the semiconductor structure recited in amended claim 41. There is no disclosure or suggestion in these references of a second portion of a semiconductor substrate formed over the cavity with at least one trench formed in the second portion adjoining the cavity. The combination of elements recited in amended claim 41 is therefore allowable and claims 42-45 are allowable for at least the same reasons as claim 41.

The present patent application is in condition for allowance. Favorable consideration and a Notice of Allowance are respectfully requested. Should the Examiner have any further questions about the application, Applicant respectfully requests the Examiner to contact the undersigned attorney at (425) 455-5575 to resolve the matter. If any need for any fee in addition to that paid with this response is found, for any reason or at any point during the prosecution of this application, kindly consider this a petition therefore and charge any necessary fees to Deposit Account 07-1897.

DATED this 27<sup>th</sup> day of February, 2006.

Respectfully submitted,

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